CLAIMS:

What is claimed is:

1. A memory array disposed above a substrate comprising:

a first plurality of spaced-apart rail-stacks disposed at a first height in a first direction above the substrate, each rail-stack including a first conductor and a first semiconductor layer extending substantially the entire length of the first conductor;

a second plurality of spaced-apart conductors disposed above the first height and in a second direction different than the first direction, and

an insulating layer disposed between the first rail-stack and the second conductors which is capable of being selectively breached by passing a current between one of the first and one of the second conductors to program the array.

2. The array defined by claim 1 wherein the first semiconductor layer is a silicon layer.

3. The array defined by claim 2 wherein the first and second conductors are perpendicular to one another.

4. The array defined by claim 3 wherein the first silicon layer is more heavily doped adjacent to the first conductor than it is at its surface spaced-apart from the first conductor.

5. The array defined by claim 4 wherein the second conductors have a second silicon layer disposed on the second conductors extending substantially the entire length of the second conductors.

6. The array defined by claim 4 wherein the insulating layer is on the surface of the first silicon layer spaced-apart from the first conductor.

7. The array defined by claim 6 wherein the second conductors are on the insulating layer.

8. The array defined by claim 7 wherein the silicon is doped with an n-type dopant.

9. The array defined by claim 8 wherein Schottky diodes are formed to program the array.

10. A memory array disposed above a substrate comprising:

a first plurality of parallel spaced-apart rail-stacks disposed above the substrate running in a first direction;

a second plurality of parallel spaced-apart rail-stacks disposed above the first rail-stacks, the second plurality of rail-stacks running in a second direction different than the first direction such that a projection of the second rail-stack on the first rail-stack define intersections with the first plurality of rail-stacks; and

a layer of low conducting material separating the first plurality of rail-stacks from the second plurality of rail-stacks, the layer of low conducting material at each intersection of the first and second rail-stacks separating a first conductivity type doped semiconductor material in one of the first rail-stacks from a second conductivity type doped semiconductor material in one of the second rail-stacks.

11. The memory array defined by claim 10 wherein the semiconductor material is silicon.

12. The memory array defined by claim 11 wherein the passage of a current equal to or greater than a predetermined threshold from one of the

first rail-stacks to one of the second rail-stacks causes a diode to form at the intersection of these rail-stacks.

13. The memory array defined by claim 12 wherein the silicon on one side of each intersection is more lightly doped than the silicon on the opposite side of each intersection.

14. The memory array defined by claim 13 wherein the side of the intersection having the more lightly doped silicon includes a more heavily doped silicon region between the more lightly doped silicon and its respective conductor.

15. The memory array defined by claims 10 or 14 wherein the low conducting material comprises silicon dioxide.

16. The memory array defined by claims 10 or 14 wherein the low conducting material layer comprises silicon nitride.

17. The memory array defined by claims 10 or 14 wherein the low conducting material layer comprises undoped silicon.

18. The memory array defined by claims 10 or 14 wherein the first and second rail-stacks include a conductor comprising a metal.

19. The memory array defined by claim 18 wherein each conductor is sandwiched between silicon in a multi-level array.

20. In a multi-level memory having alternate levels of first spaced-apart conductors extending in one direction and second spaced-apart conductors in the other levels extending in a second direction, an improvement wherein each first conductor includes:

a first layer of a first conductivity type doped semiconductor material disposed on one side of the conductor over substantially its entire length;

a second layer of the first conductivity type doped semiconductor material disposed on the opposite side of the conductor over substantially its entire length;

a third layer of the first conductivity type doped semiconductor material disposed on the second layer over substantially its entire length, the third layer being more lightly doped than the second layer; and

a dielectric disposed on the third layer.

21. The memory defined by claim 20 wherein the semiconductor material is silicon.

22. The memory defined by claim 21 wherein the dielectric is silicon dioxide.

23. The memory defined by claim 22 wherein the dielectric is silicon nitride.

24. The memory defined by claim 23 wherein the memory is programmed by forming Schottky diodes at selected intersections of the first and second conductors.

25. The memory defined by claims 20 or 21 wherein a second dielectric is disposed on the first layer.

26. The memory defined by claim 20 wherein each second conductor includes:

a fourth layer of a second conductivity type doped semiconductor material disposed on one side of the second conductor over substantially its entire length;

a fifth layer of a second conductivity type doped semiconductor material disposed on the opposite side of the second conductor over substantially its entire length;

a sixth layer of the second conductivity type doped semiconductor material disposed on the fifth layer over substantially its entire length, the sixth layer being more lightly doped than the fifth layer; and

a third dielectric disposed on the sixth layer.

27. The memory defined by claim 26 wherein the second conductivity type doped material is doped silicon.

28. In a multi-level memory having alternate levels of first spaced-apart conductors extending in one direction and second spaced-apart conductors in the other levels extending in a second direction, an improvement wherein each first conductor includes:

a first layer of a first conductivity type doped semiconductor material disposed on one side of the first conductor over substantially its entire length;

a second layer of the first conductivity type doped semiconductor material disposed on the first layer over substantially its entire length, the second layer being more lightly doped than the first layer; and

a first dielectric disposed on the second layer.

29. The memory defined by claim 28 wherein the semiconductor material is silicon.

30. The memory of claim 29 wherein the second conductors include a third layer of silicon doped with a second conductivity type dopant extending over substantially its entire length; and

a second dielectric disposed on the third layer.

31. The memory defined by claim 30 wherein additional silicon layers are disposed on the first and second dielectric.

32. A multi-level non-volatile memory array comprising:

a plurality of first rail-stacks disposed at a first and third level running generally in a first direction above a substrate, each rail-stack comprising first conductors sandwiched between layers of silicon;

a plurality of second rail-stacks disposed at a second and fourth level above the substrate and running in a second direction, each of the second rail-stacks comprising second conductors sandwiched between layers of silicon, and

a plurality of layers of dielectric each disposed respectively between successive levels of the first and second rail-stacks which are capable of being selectively breached to program the array.

33. The array defined by claim 32 wherein the layers of silicon on the first conductors are doped with a first conductivity type dopant and wherein the layers of silicon on the second conductor are doped with a second conductivity type dopant.

34. The array defined by claim 33 wherein the layers of silicon on at least one side of the first conductors are more heavily doped adjacent to the first conductor than they are further from the first conductor.

35. The array defined by claim 34 wherein the layers of silicon on at least one side of the second conductors are more heavily doped adjacent to the second conductors than they are further from the second conductors.

36. The array defined by claim 35 wherein the layer of dielectric comprises silicon dioxide.

37. The array defined by claim 35 wherein the layer of dielectric comprises silicon nitride.

38. The array defined by claim 35 wherein the first rail-stacks and second rail-stacks form right angles.

39. A multi-level non-volatile memory array comprising:

a plurality of first rail-stacks disposed at a first and third level running generally in a first direction above a substrate, each rail-stack comprising first conductors sandwiched between layers of silicon;

a plurality of second rail-stacks disposed at a second and fourth level above the substrate and running in a second direction, each of the second

rail-stacks comprising second conductors sandwiched between layers of silicon, and

a plurality of dielectric regions disposed between levels of the first and second rail-stacks which are capable of being selectively breached to program the array.

40. The array defined by claim 39 wherein the dielectric regions are grown from one of the layers of silicon.

41. A method for fabricating a multi-level memory array comprising the steps of:

depositing a metal layer;

forming at least one layer of silicon on the metal layer where the silicon is doped with a first conductivity type dopant;

masking and etching the silicon and metal layers to define a plurality of parallel, spaced-apart rail-stacks;

filling the space between the rail-stacks with a dielectric material;

planarizing the silicon layer and the dielectric material to form a planarized surface, and

forming a layer of material for an antifuse on the planarized surface.

42. The method defined by claim 41 wherein the layer of antifuse material comprises a dielectric.

43. The method defined by claim 41 wherein the layer of antifuse metal comprises undoped silicon.

44. The method defined by claim 41 wherein the layer of antifuse material is grown on the rail-stacks.

45. The method defined by claim 41 wherein the layer of antifuse material is a blanket deposition on the rail-stacks and filling material.

46. The method defined by claim 42 wherein the silicon layer comprises a first silicon heavily doped with an n-type dopant and a second layer more lightly doped with the n-type dopant.

47. The method defined by claim 42 wherein the silicon layer is a heavily doped layer.

48. The method defined by claim 47 wherein the antifuse layer is approximately 80-200Å thick and comprises silicon dioxide.

49 . A method for fabricating a multi-level memory array comprising the steps of:

forming a metal layer;

forming a first silicon layer heavily doped with a first conductivity type dopant on the metal layer;

depositing a second silicon layer on the first silicon layer, the second silicon layer being more lightly doped than the first layer with the first conductivity type dopant;

forming a layer of an antifuse material on the second silicon layer;

depositing a third silicon layer on the layer of antifuse material heavily doped with a second conductivity type dopant;

defining spaced-apart rail-stacks from the conductive layer, first and second silicon layers, the layer of antifuse material and third silicon layer;

filling space between the rail-stacks with a dielectric, and

planarizing the upper surface of the dielectric fill and the third silicon layer.

50. The method of claim 49 including repeating the steps of claim 49 to form second lines disposed above the first lines and generally perpendicular to the first lines.

51. The method defined by claim 50 including additionally etching through the third silicon layer of the first lines in alignment with the second lines.

52. A method for fabricating a multi-level memory array comprising the steps of:

forming a first silicon layer lightly doped with a first conductivity type dopant;

forming a second silicon layer on the first silicon layer, the second silicon layer being more lightly doped than the first layer with the first conductivity;

forming a layer of an antifuse material on the second silicon layer;

depositing a third silicon layer on the layer of antifuse material heavily doped with a second conductivity type dopant;

defining spaced-apart rail-stacks from the conductive layer, first and second silicon layers, the layer of antifuse material and third silicon layer;

filling between the rail-stacks with a dielectric, and

planarizing the upper surface of the dielectric fill and the third silicon layer.

53. The method defined by claim 52 wherein the layer of antifuse material is an oxide grown on the second silicon layer.

54. The method defined by claim 53 wherein the layer of antifuse material is a deposited dielectric.

55. The method of claim 52 including repeating the steps of claim 52 to form second rail-stacks disposed above the first rail-stacks perpendicular to the first rail-stacks with the conductivity type of each silicon layer reversed.

56. The method defined by claim 55 including additionally etching through the third silicon layer of the first rail-stacks in alignment with the second rail-stacks.

57. A method for fabricating a multi-level memory array comprising the steps of:

forming a first silicon layer lightly doped with a first conductivity type dopant;

forming a second silicon layer more heavily doped than the first layer with the first conductivity type dopant;

depositing a conductive layer on the second silicon layer;

depositing a third silicon layer heavily doped with a second conductivity type dopant;

etching the first, second and third silicon layers and conductive layers to define a plurality of parallel, spaced-apart rail-stacks;

filling the space between the rail-stacks with a dielectric material;

planarizing the third silicon layer and the dielectric filling material, and

depositing a layer of an antifuse material on the planarized surface.

58. The method defined by claim 57 wherein the conductive layer is approximately 500-1,500Å thick.

59. The method defined in claim 57 wherein the first silicon layer is 1000-4000Å thick.

60. The method defined in claim 57 wherein the second silicon layer is approximately 300-3000Å thick.

61. The method defined in claim 57 wherein the third silicon layer is approximately 300-2000Å thick after planarization.

62. The method defined by claim 57 wherein the antifuse layer is a silicon dioxide layer with a thickness of approximately <200Å thick.

63. The method defined by claim 57 wherein the antifuse layer is a grown silicon dioxide layer grown from the third silicon layer.

64. The method defined by claim 57 wherein the antifuse layer is a silicon nitride layer.